

## CLAIMS

1           1.       (currently amended) A circuit comprising:  
2           (a)       a set of interconnected delay stages; and  
3           (b)       switch-controlled load circuitry connected to the output of one or more delay stages,  
4 wherein the switch-controlled load circuitry substantially shields the delay stages from noise in a power  
5 supply connected to the switch-controlled load circuitry, wherein:  
6                 for each delay stage output, the switch-controlled load circuitry (1) is connected between  
7 the power supply and the delay stage output and (2) comprises a current source, a load, and a switch,  
8 wherein the switch is adapted to selectively apply the load to the delay stage output;  
9                 the load corresponds to a gate-to-channel capacitance of a transistor; and  
10                the transistor is connected to the switch at a transistor gate node and to the current source  
11 at a first transistor channel node.

1           2.       (original) The invention of claim 1, wherein the switch-controlled load circuitry is  
2 connected to the output of each delay stage.

1           3.       (original) The invention of claim 1, wherein the switch-controlled load circuitry  
2 selectively applies a load to the corresponding delay stage output.

1           4.       (canceled)

1           5.       (original) The invention of claim 1, wherein the circuit is an oscillator and the plurality  
2 of delay stages are connected in a ring.

1           6.       (original) The invention of claim 5, wherein the oscillator is a voltage-controlled  
2 oscillator, wherein the gain of each delay stage is a function of an applied control voltage.

1           7.       (canceled)

1           8.       (currently amended) The invention of claim [[7]] 1, wherein the impedance of the  
2 current source substantially decouples the load from the power supply.

1           9.       (currently amended) The invention of claim [[7]] 1, wherein the current source is a  
2 constant current source.

1           10-11. (canceled)

1           12.       (currently amended) The invention of claim [[11]] 1, wherein a second transistor  
2 channel node is connected to local ground.

1           13.       (currently amended) The invention of claim [[11]] 1, wherein the first transistor channel  
2 node is the transistor source.

1           14.       (currently amended) The invention of claim [[11]] 1, wherein:  
2 the gate-to-channel capacitance corresponds to the gate-to-source capacitance of the transistor;  
3 the current drain is connected to the transistor source; and  
4 the transistor source is connected to local ground.

1 15. (currently amended) The invention of claim [[11]] 1, wherein the transistor is an NMOS  
2 transistor.

1 16. (currently amended) The invention of claim [[7]] 1, wherein:  
2 each switch is adapted to be closed when an operating frequency of the circuit is below a  
3 specified threshold frequency; and  
4 each switch is adapted to be open when the operating frequency of the circuit is above the  
5 specified threshold frequency.

1 17. (currently amended) The invention of claim 1, wherein:  
2 the switch-controlled load circuitry is connected to the output of each delay stage;  
3 the switch-controlled load circuitry selectively applies a capacitive load to the corresponding  
4 delay stage output;  
5 the circuit is a voltage-controlled oscillator and the plurality of delay stages are connected in a  
6 ring, wherein the gain of each delay stage is a function of an applied control voltage;  
7 ~~for each delay stage output, the switch-controlled load circuitry (1) is connected between the~~  
8 ~~power supply and the delay stage output and (2) comprises a current source, a load, and a switch,~~  
9 ~~wherein the switch is adapted to selectively apply the load to the delay stage output;~~  
10 the impedance of the current source substantially decouples the load from the power supply;  
11 the load corresponds to a gate-to-channel capacitance of a transistor;  
12 ~~the transistor is connected to the switch at a transistor gate node and to the current source at a~~  
13 ~~first transistor channel node;~~  
14 each switch is adapted to be closed when an operating frequency of the circuit is below a  
15 specified threshold frequency; and  
16 each switch is adapted to be open when the operating frequency of the circuit is above the  
17 specified threshold frequency.

1 18. (original) A voltage-controlled oscillator comprising:  
2 (a) a set of interconnected delay stages; and  
3 (b) switch-controlled load circuitry connected to the output of one or more delay stages,  
4 wherein the switch-controlled load circuitry includes a transistor, a switch connected between a delay  
5 stage output and a gate node of the transistor, and a current source connected between a power supply for  
6 the transistor and a channel node of the transistor.

1 19. (original) The voltage-controlled oscillator of claim 18, wherein the transistor is an  
2 NMOS transistor, the current source is connected to the drain node of the NMOS transistor, and the load  
3 corresponds to the gate-to-source capacitance of the NMOS transistor.

1 20. (original) The voltage-controlled oscillator of claim 18, wherein the current source  
2 comprises a PMOS transistor.

1 21. (original) A voltage-controlled oscillator comprising:  
2 (a) a set of interconnected delay stages;  
3 (b) a switch-controlled load connected to the output of one or more delay stages; and  
4 (c) means for shielding the delay stages from noise in a power supply connected to the  
5 switch-controlled load.